IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A microprocessor comprising:

a cache memory;

an instruction processor[,]coupled to receive instructions from said cache memory;

an instruction decoder to decode the output from said instruction processor[,]; and

a processor to make calculations according to the output from said instruction decoder,

wherein, when the instructions that are input from the cache memory are specified instructions, said instruction processor outputs said input instructions to said instruction decoder, and when the input instructions are other than said specified instructions, a first instruction different from said input instructions is output from said instruction processor to said instruction decoder.

2. (Original) A microprocessor according to claim 1, wherein said instruction processor has an instruction discriminator circuit and an instruction selector circuit, and said discriminator circuit determines whether or not the instruction input into said instruction processor is said specified instruction, and based on said discrimination results, said instruction selector circuit selects either

said first instruction or said input instruction and outputs either said first instruction or said input instruction to said instruction decoder.

3. (Original) A microprocessor according to claim 1 or claim 2, wherein said specified instruction is an instruction to perform calculations in said processor.

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4. (Previously Presented) A microprocessor according to claim 1 or claim 2, wherein said first instruction is an NOP instruction.

5. (Previously Presented) A microprocessor according to claim 1 or claim 2, wherein said first instruction is an instruction for a designated code.

6. (Previously Presented) A microprocessor according to claim 1 or claim 2, wherein said processor is a processor for a designated processing circuit.

7. (Original) A microprocessor according to claim 6, wherein said designated processor is a floating point unit.

8. (Previously Presented) A microprocessor according to claim 1 or claim 2, wherein said processor calculates the data stored in a first latch and outputs said calculated results to a second latch, and the supply of clock pulses to said first latch and said second latch is halted when said first instruction is input to said instruction decoder.

9. (Currently Amended) A microprocessor according to claim 1 or claim 2, further comprising a ~~second~~ register to receive instructions, a second instruction decoder connected to said ~~second~~ register, and a second processor controlled by the output of said second instruction decoder, wherein the instruction supplied to said instruction processor ~~circuit~~ and the instruction input to said ~~second~~ register are the same instruction.

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10. (Previously Presented) A microprocessor according to claim 1 or claim 2, wherein said microprocessor is formed on the same semiconductor substrate.

11. – 31. (Cancelled)

32. (Currently Amended) A microprocessor comprising:

a cache memory

an instruction processor circuit[~~,~~] coupled to said cache memory;

a first decoder to decode the output of said instruction processor circuit~~,~~;

a first processor to make calculations according to the decoding results from said first decoder~~,~~;

a second decoder to decode the output from said instruction processor circuit~~,~~; and

a second processor to make a calculation according to decoding results from said second decoder,

wherein, when the instruction that is input from said cache memory is not ~~the~~an instruction to perform calculations in said second processor, ~~an~~said instruction

~~is output~~processor circuit outputs the instruction that is input from said cache memory and an instruction ~~for said second decoder~~ that is different from the instruction that is input from said cache memory to said second decoder.

33. (Original) A microprocessor according to claim 32, wherein said different instruction is an NOP instruction.

34. (Original) A microprocessor according to claim 32 or claim 33, wherein said first processor is an arithmetic logic unit, and said second processor is a processor with a designated calculator circuit.

35. (Original) A microprocessor according to claim 34, wherein said designated calculator circuit is an FPU.

36. (Previously Presented) A microprocessor according to claim 32 or claim 33, wherein said second processor calculates the data stored in the first latch, and outputs the calculation results to the second latch and, when the instruction input to said instruction processor circuit is not the instruction to perform calculation in said second processor, said instruction processor circuit stops the supply of clock pulses to said first latch and to said second latch.

37. (Previously Presented) A microprocessor according to claim 32 or claim 33, wherein when the instruction input to said instruction processor circuit is

not the instruction to perform calculation in said first processor, said instruction processor circuit does not output said input instruction to said first decoder.

38. (Previously Presented) A microprocessor according to claim 32 or claim 33, wherein said microprocessor is formed on the same semiconductor substrate.

39. – 51. (Cancelled)

52. (Currently Amended) A microprocessor comprising:

a cache memory;

an instruction processor circuit input with instructions[,] from said cache memory;

a instruction decoder input with the output of said instruction processor circuit,; and

a processor to make calculations according to decoding results from said instruction decoder,

wherein said instruction processor circuit has a selector circuit to select either a first instruction different from the input instruction or said input instruction, and a discriminator circuit input with a specified bit of said input instruction, and

wherein, when said specified bit is a first status, said discriminator circuit controls said selector circuit and outputs said first instruction to said instruction decoder, and

wherein, when said specified bit is not a first status, said discriminator circuit controls said selector circuit to output said input instruction to said instruction decoder.

53. (Cancelled)

54. (Original) A microprocessor according to claim 52 or claim 53, wherein said first instruction is an NOP instruction.

55. (Original) A microprocessor according to claim 52 or claim 53, wherein said first instruction is a designated code.

56. (Previously Presented) A microprocessor according to claim 52 or claim 53, wherein said processor is the processor of a designated calculation circuit.

57. – 62. (Cancelled)